Realization of Gates (Transistor as Switch)

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Outline

- Digital Logic States
- Transistor as a Switch
  - Transistor in Cut Off
  - Transistor in Saturation

Digital Logic States (cont…)

Most *digital logic gates* and digital logic systems use "**Positive Logic**", in which a logic level "0" or "LOW" is represented by a **zero voltage**, **0V or ground** and a logic level "1" or "HIGH" is represented by a higher voltage such as **+5 volts.**

Boolean Algebra	Boolean Logic	Voltage State	Voltage Level
Logic "1"	TRUE (T)	HIGH (H)	~ +5V
Logic "0"	FALSE (F)	LOW (L)	~ 0V

However, when using a standard +5 volt supply **any voltage input between 2.0V and 5V** is considered to be a logic "1" or "HIGH" while **any voltage input below 0.8V** is recognised as a logic "0" or "LOW".
The voltage region in between these two voltage levels either as an input or as an output is called the *Indeterminate Region* and operating within this region may cause the logic gate to produce a false output.

Realization of Gates

The digital logic gates can be made by different combinations of transistors (T), diodes (D) and resistors (R).

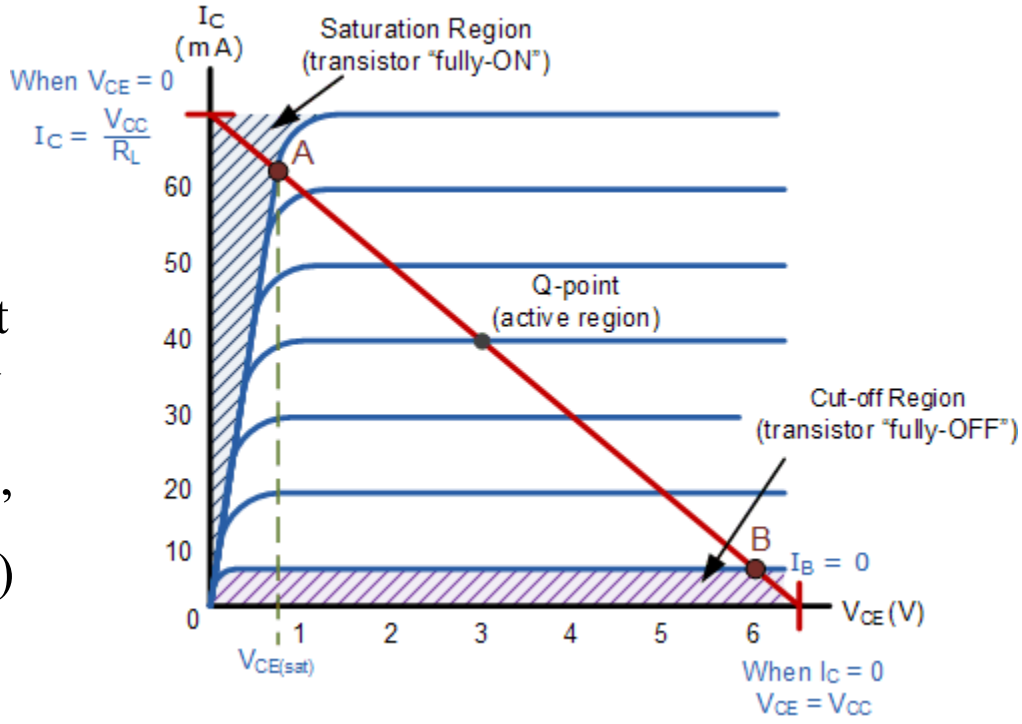
There are different advantages and disadvantages of these combinations.

We will study few of these combinations in detail, but before that we will recap the **transistor as a switch**.

Transistor as Switch

For the transistor as a switch the areas of operation are **Saturation Region** and the **Cut-off Region**.

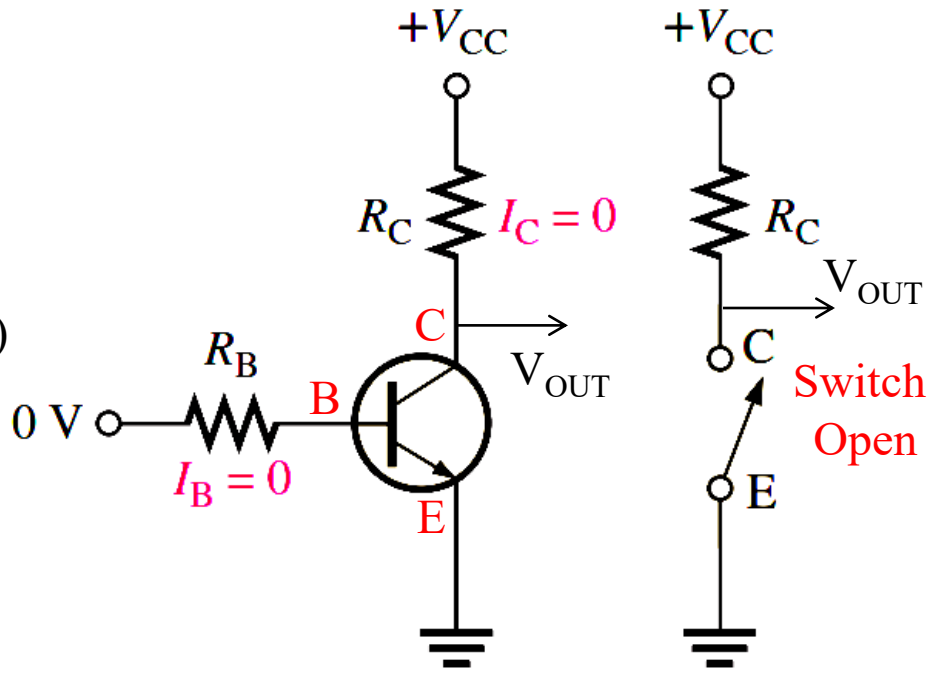
We can ignore the operating Q-point biasing and voltage divider circuitry and use the transistor as a switch by driving it in between its “fully-OFF” (cut-off) and “fully-ON” (saturation) regions.



I-V Characteristics

Transistor in Cut-off Region

- The input and Base are grounded (0V)
- Base-Emitter voltage $V_{BE} < 0.7V$
- Base-Emitter junction is reverse biased
- Base-Collector junction is reverse biased
- Transistor is "fully-OFF" (Cut-off region)
- No Collector current flows ($I_C = 0$)
- $V_{OUT} = V_{CE} = V_{CC} = 1$
- Transistor operates as an "**Open Switch**"



Transistor in Saturation Region

- The input and base are connected to V_{CC}
- Base-Emitter voltage $V_{BE} > 0.7V$
- Base-Emitter junction is forward biased
- Base-Collector junction is forward biased
- Transistor is "fully-ON" (saturation region)
- Max Collector current flows ($I_C = Vcc/R_C$)
- $V_{CE} = 0$ (ideal saturation)
- $V_{OUT} = V_{CE} = 0$
- Transistor operates as a "**Closed Switch**"